

700-V Asymmetrical 4H-SiC Gate Turn-Off Thyristors (GTO's)

A. K. Agarwal, *Member, IEEE*, Jeffrey B. Casady, *Member, IEEE*, L. B. Rowland, S. Seshadri, R. R. Siergiej, W. F. Valek, and C. D. Brandt

Abstract—Silicon Carbide (4H-SiC), asymmetrical gate turn-off thyristors (GTO's) were fabricated and tested with respect to forward voltage drop (V_F), forward blocking voltage, and turn-off characteristics. Devices were tested from room temperature to 350 °C in the dc mode. Forward blocking voltages ranged from 600–800 V at room temperature for the devices tested. V_F of a typical device at 350 °C was 4.8 V at a current density of 500 A/cm². Turn-off time was less than 1 μ s. Although no beveling or advanced edge termination techniques were used, the blocking voltage represented approximately 50% of the theoretical value when tested in an air ambient. Also, four GTO cells were connected in parallel to demonstrate 600-V, 1.4 A (800 A/cm²) performance.

I. INTRODUCTION

SILICON CARBIDE (SiC) has long been known to possess significant material advantages (higher thermal conductivity, higher breakdown field, wider bandgap, and higher saturated electron drift velocity) in comparison to Si and GaAs for high-power switching applications [1]–[4]. Although large-area devices are yet to be fully realized because of limited material development, SiC power devices have now been fabricated with promising performance. SiC power devices fabricated include pn junction and Schottky diodes, thyristors, UMOFET's, JFET's, and SIT's [1], [5]. Power MOSFET's have been reported with blocking voltages of 760 V and low on-resistance (66 m Ω · cm²) [4]. Symmetrical thyristors with blocking voltages of 900 V and on-state currents of 2.0 A have been reported, as well as larger-area thyristors with 700 V, 6.0 A performance [3]. The 700 V device had V_F of 3.67 V at a current density of 1000 A/cm². These devices also demonstrated reliable operation after 600 h storage at 400 °C in an air ambient. SiC power devices such as thyristors and pn junction diodes should be capable of high operating temperatures (500 °C), eliminating costly, expensive, and bulky cooling systems. Because of SiC's high breakdown strength (\sim 2.3 MV/cm [1]), faster-switching power devices as well as ultra-high voltage devices in the range of 40 kV should be feasible. In this work, we report the fabrication and characterization of asymmetrical 4H-SiC Gate Turn-Off Thyristors (GTO's). The GTO structure has advantages over the conventional thyristor in that it can be turned off with a gate pulse, allowing it to be used in dc power switching

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The authors are with the Northrop Grumman Science and Technology Center, Electronic Sensors and Systems Division, Pittsburgh, PA 15235-5080 USA.

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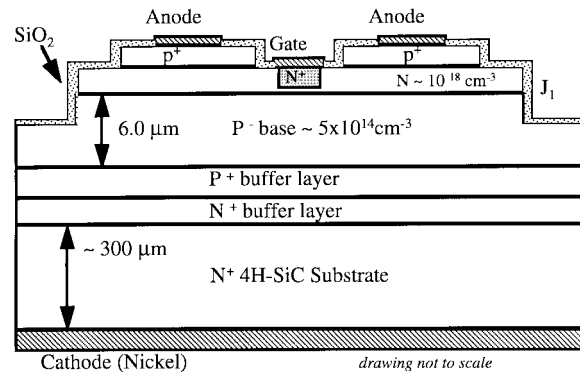


Fig. 1. Inverted, asymmetrical 4H-SiC GTO device cross section. The forward blocking junction (anode positive) is labeled J1.

since it does not require the negative ac cycle for turn-off. The asymmetrical GTO structure also has the advantage of easier turn-off in comparison to symmetrical devices. Additionally, the asymmetrical GTO structure is less susceptible to open base transistor breakdown which generally determines the breakdown voltage in conventional thyristors. Also, unlike the SiC power MOSFET, IGBT, and MCT devices, the GTO does not have the reliability problems of a dielectric subject to high electric fields at high temperatures [6], [7]. Thus, the asymmetrical SiC GTO represents a promising high-power device for good high-temperature reliability, fast switching, and sensitive turn-on and turn-off control.

II. DEVICE STRUCTURE AND FABRICATION

A cross section of the asymmetrical GTO is shown in Fig. 1. Because of the partial ionization of p-type acceptor impurities in SiC, it is difficult to obtain highly-conductive p-type SiC substrates. To counter this, the structure was inverted and fabricated on a heavily doped (1×10^{19} cm⁻³), 12 mil thick, n-type, Si-face, 8° off-axis, 4H-SiC substrate. Five epitaxial layers were grown on the substrate. First, an n⁺ buffer layer was grown. Next, a heavily doped p-type buffer layer was epitaxially deposited in order to form a punch-through structure and also to allow easier turn-off of the device by reducing the injection efficiency of the bottom npn bipolar transistor. The blocking voltage is supported across a lightly doped (\sim 5 \times 10¹⁴ cm⁻³) 6.0- μ m thick p-type base layer. Finally, n-type gate and p-type anode epitaxial layers were grown. The forward blocking (anode positive) junction (J1) is also shown in Fig. 1. The anode isolation and edge termination were both accomplished via reactive ion etching

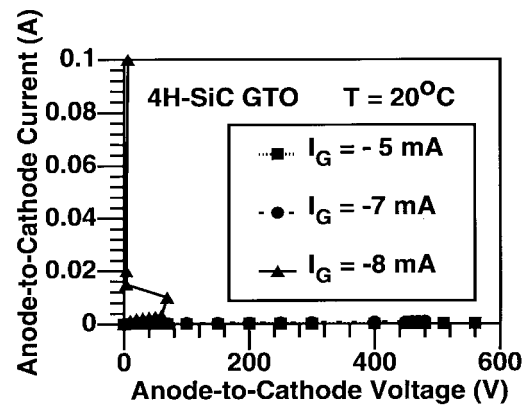
in CHF_3 , H_2 , and O_2 . High-temperature nitrogen implantation (similar to [8]) was performed under the gate contact area to reduce the gate contact resistance. A combination of thermal and deposited silicon dioxide layers was used to passivate the mesa edge termination of the device. Nickel silicide ohmic contacts were used for the gate and cathode [9] resulting in an ohmic contact resistance of $5 \times 10^{-4} \Omega \cdot \text{cm}^2$ from TLM measurements, while an aluminum-titanium alloy was used for the p^+ anode contact [10]. Interdigitated anode and gate fingers were of equal lengths and widths for these nonoptimized, first-generation devices. Typical finger lengths and widths were 250 and 15 μm , respectively.

III. EXPERIMENTAL RESULTS AND DISCUSSION

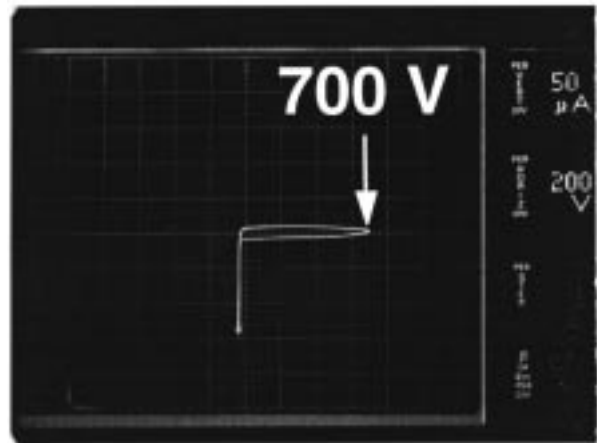
The 4H-SiC GTO's exhibited forward blocking in the range of 600–800 V for most of the devices tested. Testing was performed on a high-temperature probe station in an air ambient, similar to that performed on other SiC thyristors [3], [11], without the use of FluorinertTM. The dc turn-on characteristics of a typical GTO are shown in Fig. 2(a) as measured with gate currents of -5 , -7 , and -8 mA to illustrate the sensitive turn-on of the device. With no gate current, the forward blocking voltage of a typical device (700 V) is shown in Fig. 2(b).

This blocking voltage corresponded to a maximum electric field (E_m) of approximately 1.2 MV/cm across the blocking layer for a nominal 700-V blocking device when assuming negligible voltage drop across the anode, substrate, contacts, and buffer layers. This value of E_m is about 50% of the theoretical critical electric field possible in 4H-SiC [1]. Emissions of light at the periphery of the device structure in breakdown were observed under high-power ($50\times$) magnification in the dark, consistent with edge-breakdown. Further improvements in edge termination should improve the breakdown characteristics of the devices. For comparison purposes, it is notable that for punch-through structures in silicon such as a p-n diode, a 45- μm thick blocking layer of equal doping would be necessary to achieve the same 600-V blocking as with the 6- μm SiC blocking layer used here [12]. The dramatic reduction in the required blocking layer thickness for this device structure utilizing SiC's high electric breakdown strength should allow for much faster power switching than conventional silicon devices.

Forward voltage drops at different temperatures were measured as well, and are shown as a function of current density from a typical device in Fig. 3. V_F ranged from 4 to 10 V for typical devices depending upon current density. At high current densities, the forward drop is significantly increased from the high anode contact resistance ($7 \times 10^{-3} \Omega \cdot \text{cm}^2$ as measured from TLM) and future efforts are concentrating on lowering the anode contact resistance to improve device performance. Maximum current densities of up to 2500 A/cm² were obtained in some devices, but current was limited in obtaining Fig. 3 to avoid premature device failure. V_F decreases at higher operating temperatures for two reasons. First, because of increased carrier ionization in SiC (in particular the p-type layers) the resistivity of the semiconductor is decreased. Second, from the ideal diode equation, the voltage



(a)



(b)

Fig. 2. (a) Typical forward current-voltage characteristics of a 4H-SiC GTO with dc gate currents of -5 , -7 , and -8 mA. (b) Forward blocking voltage of a typical 4H-SiC GTO, measured in an air ambient without FluorinertTM.

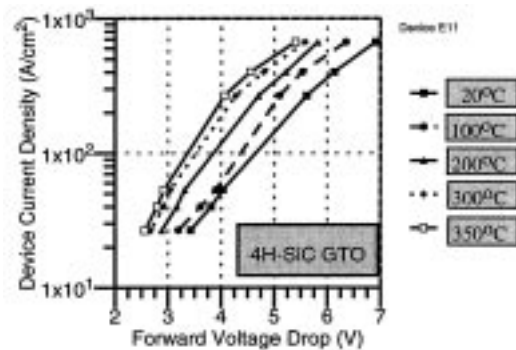


Fig. 3. Forward voltage drop as a function of current density and temperature for a typical 4H-SiC GTO. Current density was normalized to anode area.

drop across a pn junction at a constant current decreases with temperature (by 2.24 mV/°C in 6H-SiC) because of the exponential increase in intrinsic carrier concentration with increasing temperature [13]. A forward drop of 4.8 V was measured at 500 A/cm² (normalized to the anode area) at a temperature of 350 °C for a typical device. The forward drop may be marginally increased as a result of the p^+ buffer layer inserted to increase the turn-off gain by decreasing the injection efficiency of the bottom npn transistor.

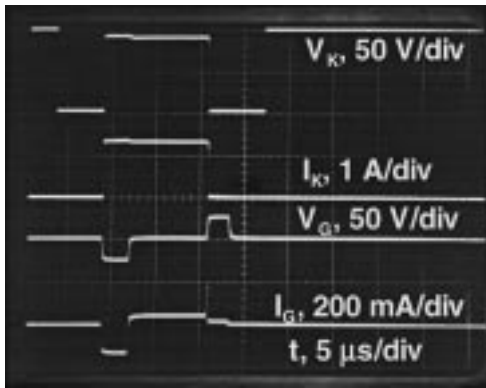


Fig. 4. Pulsed characteristics of four packaged, parallel GTO devices. The top trace represents the cathode-to-anode voltage, and the second trace from top represents the cathode-to-anode current. The third and fourth traces from the top represent the gate voltage and current, respectively used to run the device on and off. These four cells in parallel demonstrated 600 V, 1.4 A performance.

Although these device structures were nonoptimized, four identical cells were placed in parallel to demonstrate a 600 V, 1.4 A device as shown in Fig. 4, which would correspond to 800 A/cm² assuming uniform current distribution between devices. The top trace represents the cathode-to-anode voltage (V_K) which is approximately -100 V in the off-state, dropping to less than -10 V (-3.5 to -10 V) in the on-state. The second trace from the top is the anode current of the device, which conducts 1.4 A when the device is on. The third and fourth traces from the top represent the gate voltage and current, respectively. The device is turned on with a gate pulse of approximately -110 mA, and the device is turned off with a gate current pulse of approximately 200 mA. The turn-off time in all devices was extremely fast ($<1\mu\text{s}$) in comparison to Si GTO's. The turn-off time could not be accurately measured below $1\mu\text{s}$ due to the resolution of the pulse system used, but turn-off time is currently being measured in a more elaborate set-up, and will be reported on shortly. The turn-off gain (β) was measured by taking the ratio of anode current to gate current [14]. β was measured to be between three and seven for the devices tested. The maximum turn-off gain [β_m —defined by (1)] can be enhanced by reducing the injection efficiency of the bottom npn transistor in the GTO

$$\beta_m = \frac{\alpha_{\text{PNP}}}{(\alpha_{\text{PNP}} + \alpha_{\text{NPN}} - 1)}, \quad (1)$$

It is from (1) that the advantage of the p^+ buffer layer is most easily seen, since it acts to reduce the injection efficiency (and thus the base transport factor) of the bottom npn transistor. Although decreasing α_{NPN} increases β_m , one disadvantage is that it also acts to increase V_F .

IV. CONCLUSIONS

Asymmetrical 4H-SiC GTO's have been fabricated and characterized for the first time. Current densities in excess of 1000 A/cm² were easily obtained, in addition to forward

blocking voltages of 600–800 V using a $6\text{-}\mu\text{m}$ thick p-type ($N_A \sim 5 \times 10^{14} \text{ cm}^{-3}$) blocking layer. Four cells packaged in parallel were able to provide 600 V, 1.4 A performance up to temperatures of 350 °C. Excellent turn-on and turn-off characteristics were noted with a turn-off time of less than $1\mu\text{s}$ and a turn-off gain of 3–7 measured for typical devices. V_F ranged from 4 to 10 V for these unoptimized devices, with a typical 4.8-V forward drop measured at a temperature of 350 °C and a current density of 500 A/cm², normalized to the anode area.

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